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EXAMINER	
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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/878,401
Filing Date: June 12, 2001
Appellant(s): PARK, JAE YONG

Park
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 03/22/06 appealing from the Office action mailed 10/18/05.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,774,872	KAWADA	8-2004

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawada et al. (Patent No. US 6,774,872).

Regarding claims 1 and 11, Kawada teaches an electro-luminescence display (col. 1, lines 64-67) comprising:

an electro-luminescence panel having a first surface including a display area (15) and an opposite face having a non-display area (11) (fig. 4c);

driving circuit boards (23) for applying driving signals to a gate line and a data line provided on the opposite face having the non-display area of the electro-luminescence panel; and

tape carrier packages (21a') connecting the driving circuit boards (23) and the electro-luminescence panel (11) (from col. 4, line 56 to col. 5, line 10).

Kawada differs from claims 1 and 11 in that he does not specifically teach the tape carrier packages connecting the driving circuit boards and the electro-luminescence panel in a planar state. However, Kawada teaches the display device is a flat display device (col. 1, lines 9-11); accordingly, the tape carrier packages connecting the driving circuit boards and the electro-luminescence panel are generally flat. Therefore, it would have been obvious to obtain the tape carrier packages connecting the driving circuit boards and the electro-luminescence panel in a planar state in order to provide a display that is capable of being made having a small thickness.

Regarding claims 2 and 6, Kawada teaches the driving circuit boards include: a gate driving circuit for applying driving signals to the gate lines; and a data driving circuit for applying driving signals to the data lines (inherently in a electro-luminescence panel, col. 1, lines 9-52).

Regarding claim 3, Kawada further teaches the driving circuit boards (23) include a plurality of output pads (i.e., the contact area between driving circuit board 23 and one end of the TCP 21a') electrically connected to the tape carrier packages (21a') (fig. 4c).

Regarding claim 4, Kawada further teaches the EL panel includes a plurality of input pads (i.e. , ., the area near the other end of the TCP 21a') that are provided at the non-display area and electrically connected to the tape carrier packages (21a') (Fig. 4c, from col. 4, line 56 to col. 5, line 10).

Regarding claim 5, same as claims 3 and 4.

Regarding claim 6, Kawada teaches the electro-luminescence display wherein the tape carrier packages includes:

a first group of tape carrier packages arranged between the electro-luminescence panel and the gate driving circuit; and a second group of tape carrier packages arranged between the electro-luminescence panel and the data driving circuit (inherently teaches in the electro-luminescence display).

Regarding claim 7, Kawada further teaches the tape carrier packages (21a') has a first side for connecting the driving circuit boards (23) to the panel (11) and a second side for holding a computer chip (IC 21) (Fig. 4C, from col. 4, line 56 to col. 5, line 10).

Regarding claim 8, Kawada further teaches a substantial portion of each of said tape carrier packages (21a') is in a common plane with said driving circuit boards (23) (fig. 4c).

Regarding claim 9, Kawada further teaches a substantial portion of each of said tape carrier packages (21a') having a first portion disposed in a common plane with said driving circuit boards (23) and connected to the electro-luminescence panel (11) (fig. 4c).

Regarding claim 10, Kawada further teaches and a second portion disposed in a contiguous plane to the common plane of said panel and said first portion (from col. 4, line 56 to col. 5, line 10).

(10) Response to Argument

In response to Applicants' argument that because Kawada does not disclose such a planar state feature, and because no objective factual evidence has been provided to show such a feature. The rejection is based on improper speculation and/or improper hindsight reconstruction of Appellant's claimed invention based solely on Appellant's disclosure. Examiner respectfully disagrees. The planar state is *generally flat*. Kawada teaches the electro-luminescence device is a flat display panel; accordingly, the tape carrier packages connecting the driving circuit boards and the electro-luminescence panel are generally flat or in planar state. Moreover, the heat sink is not necessary mounted directly to the substrate 12, it may be contiguous with the panel thus the temperature rise of the driver circuit is effectively suppressed (figs. 4a, 4b, and 4d). It would have been an obvious matter of design choice to relocate the heat sink to be contiguous with the panel, since such a modification would have involved a mere change in relocate of a component because this would not alter the operation and / or function of the device. Relocation is generally recognized as being within the level of ordinary skill in the art. In addition, the relocation of a well-known element is normally not directed toward patentable subject matter, *In re Japikse*, 86 USPQ 70 (CCPA 1950).

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Jennifer Nguyen
6/20/06

Conferees:

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